
Radiation Tolerant SRAM for SPACE Applications

Introduction

The purpose of this document is to analyse the selection criteria for memory chips to be used in Spacecraft computers.

A general trend is to implement more autonomous functions in Spacecraft, making use of increased processor performances, but requiring larger embedded flight software sizes and larger storage on board.

This note provides an introduction to the current organisation of European Spacecraft On-Board Data Handling systems and identifies the criticality of Spacecraft computer based functions.

It recalls the constraints on memory planes linked to the Space environments, and gives examples of memory banks designs for typical sizes.

In order to introduce the context of Space projects, the following figure represents a logic flow diagram of a typical Phase A /Phase B for a Spacecraft, where the most important trade-offs in term of Data Handling architecture and components selection have to be performed.

Both Hardware and Software activities are represented, due to a strong interaction of both designs necessary to achieve the most appropriate processing system. Design of current Spacecraft on board data handling subsystems.

Starting from an approved mission concept, the Spacecraft has to be designed to meet a number of operational and environmental constraints.

A preliminary On-Board Data Handling architecture is defined, based on the experience gained by the industry, with a parallel allocation of hardware and software functions.

This phase A work relies on existing hardware, re-utilisation of standard functions and typical software figures.

The software functions are then detailed to size more precisely the necessary resources to fulfil the Spacecraft mission, and an interactive work at subsystem level is necessary to match hardware and software functions.

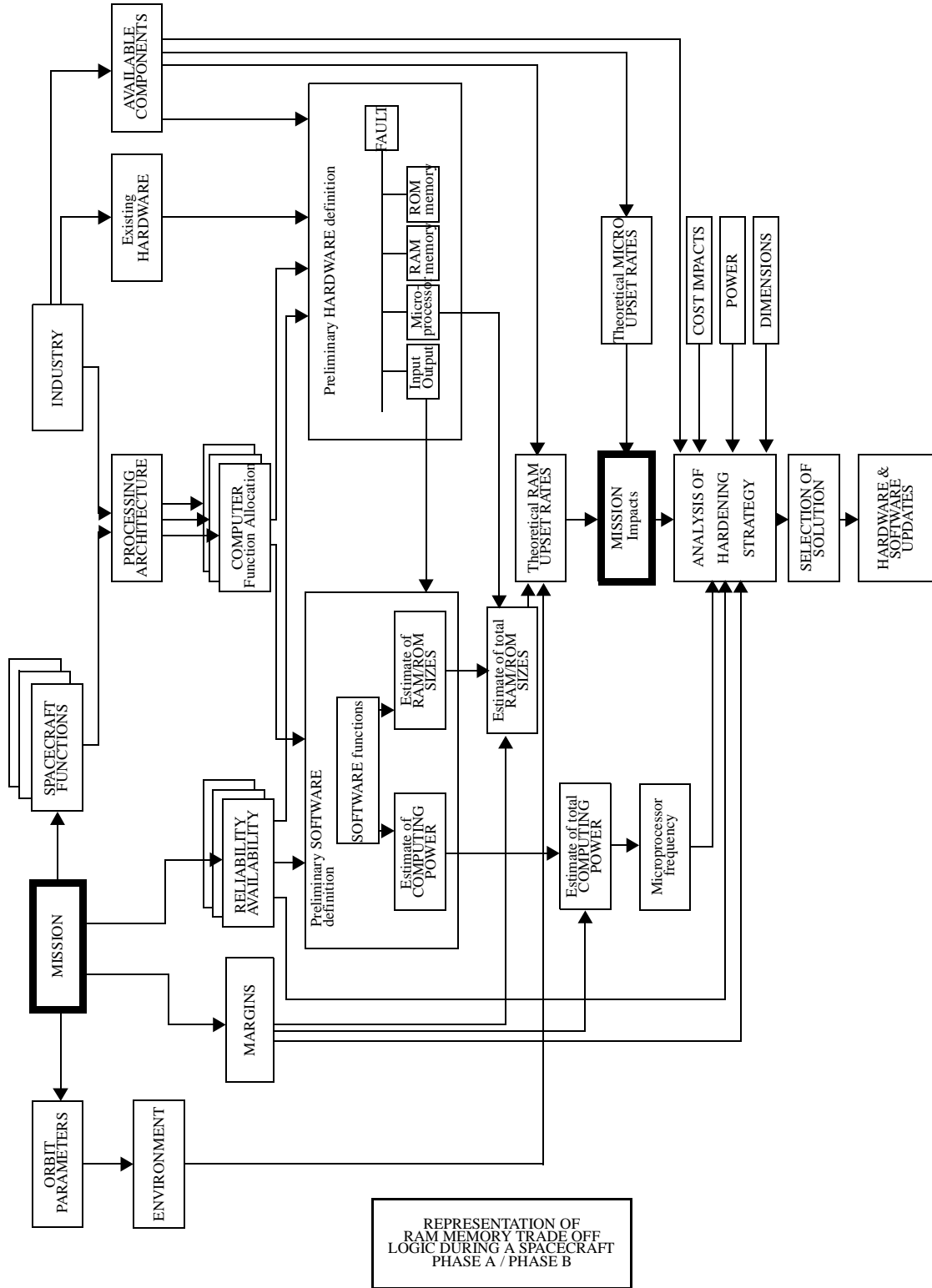
The Spacecraft design is then reviewed at system level to check that it will meet the mission objectives, especially taking into account Space environment.

Issues are then identified (mass, reliability, thermal aspects...) and corrective actions taken as necessary for each equipment or subsystem.

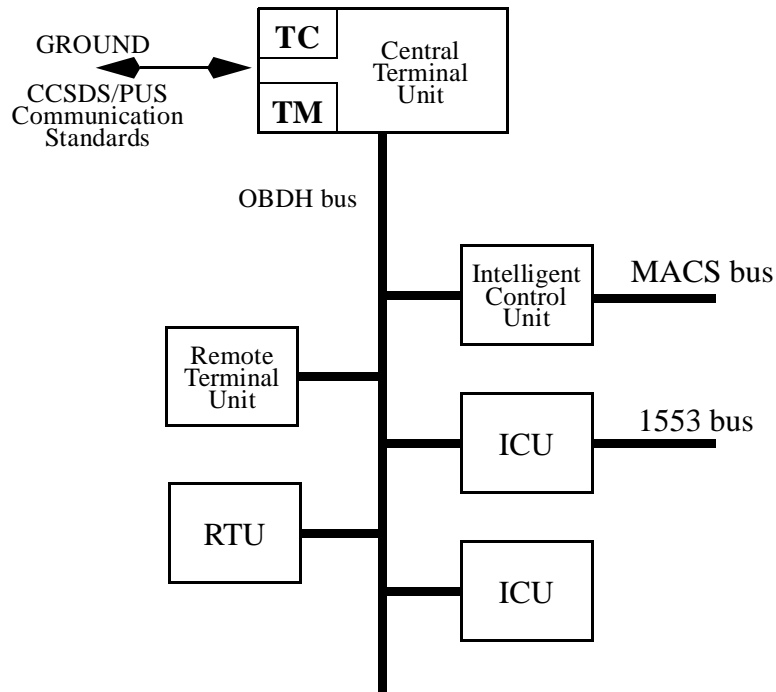
For that concern RAM banks, they have a particular importance at system level, since they contain most of flight software functions. Single event upsets have now been identified since early 80s and corrective hardware methods have been implemented to avoid catastrophic effects. The main effect remains some degradation of the Spacecraft availability, whose impacts on the mission have to be assessed.

To summarize, the following steps in the selection process for memories in Space applications to select the appropriate memory devices are:

- PRELIMINARY ARCHITECTURE
- SIZING OF COMPUTER RESOURCES
- ANALYSIS OF SEU EFFECTS ON MISSION
- HARDENING STRATEGY



The following figure shows the most general architecture for a European Spacecraft:



A Central Terminal Unit interfaces with the Telecommunication subsystem and drives the Spacecraft bus on which terminals are computers (ICU for Intelligent Computer Units dedicated to the management of an instrument or to the Spacecraft Attitude and Orbit Control) or acquisition Units (such as the RTU, remote Terminal Units).

A certain level of standardisation has been achieved in the data transfer on-board and between the Ground and Flight segments.

On-Board, data transfer buses are mainly the ESA On-Board Data Handling (OBDH) standard or 1553 bus. A specific bus for Attitude and Orbit Control subsystems (MACS bus) is also used.

Communication systems for spacecraft follow the recommendations of the CCSDS (Consultative Committee for Space Data Systems). This ensures a certain level of inter-operability between the main International Space Organisations.

This architecture can be now considered as stable, with a number of Space qualified ASICs supporting the protocols.

The allocations of functions in a Spacecraft are also nearly standardised.

The functions are generally split according to the following hierarchy:

Table 1.

Location	Type of Computer	Typical Functions
Spacecraft Bus	Central Computer	Ground-Board interface Operational sequences storage and execution Telemetry storage during non visibility periods
	Attitude and Orbit Control Subsystem Computer	Interface with the Central Computer Spacecraft Manoeuvres execution S/C attitude control laws AOCS monitoring and re-configuration Survival/safety mode attitude
Payload	Payload Controller	Interface with the Central Computer Payload operational sequences storage and execution Payload monitoring Scientific Telemetry storage
	Instrument processors	Signal or image processing Data compression Instrument or equipment activation or positioning control loops

As a general trend, data storage becomes more decentralised, especially in the Payload controllers, due to a change in the Telemetry system organisation. In previous systems, the TM bandwidth allocation used to be fixed, the telemetry system was based on a cyclic acquisition scheme within the Spacecraft.

Packet Telemetry systems nowadays allow a dynamic bandwidth allocation, which implies storage requirements for the computers generating the source packets.

As a general trend for European Spacecraft, the availability of Space qualified component in Europe for the 90s should show the following type of computers.

Table 2.

Location	Type of Computer	Typical Components
Spacecraft Bus	Central Computer	Processor Mil Std 1750 (MAS 281, MA 31750...) Memory 128 to 256 Kbytes
	Attitude and Orbit Control Subsystem Computer	Processor Mil Std 1750 (MAS 281, MA 31750...) Memory 128 Kbytes

Table 2.

Location	Type of Computer	Typical Components
Payload	Payload Controller	Processor Mil Std 1750 (MAS 281, MA 31750...) Memory 128 Kbytes
	Instrument processors	Digital Signal Processors Motorola 68xxx Microcontrollers 80Cxxx variable memory sizes

A typical example of such a Spacecraft is the XMM satellite, whose Data Handling Architecture should be close to the following one:

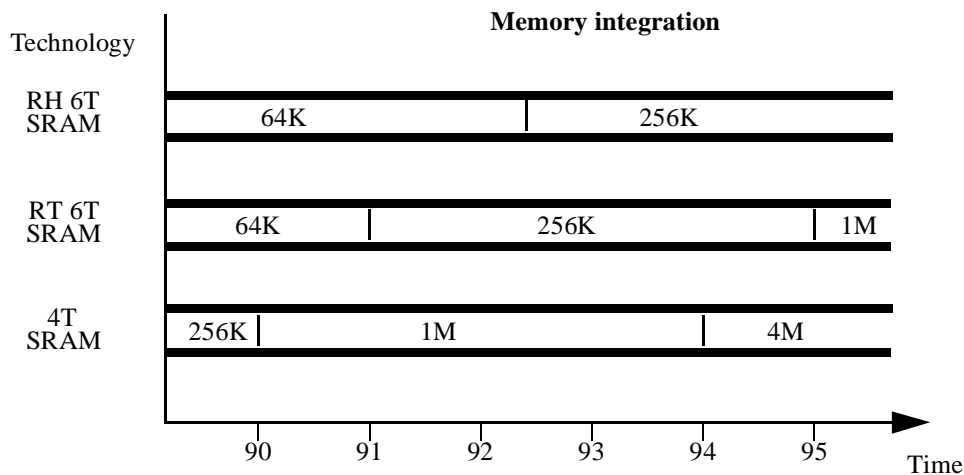
These are current data, and one can predict the use of RISCs for re-entry vehicles as well as Digital Signal Processors for Guidance, Navigation and Control associated with image processing. The following computer configurations can be considered as typical for space applications:

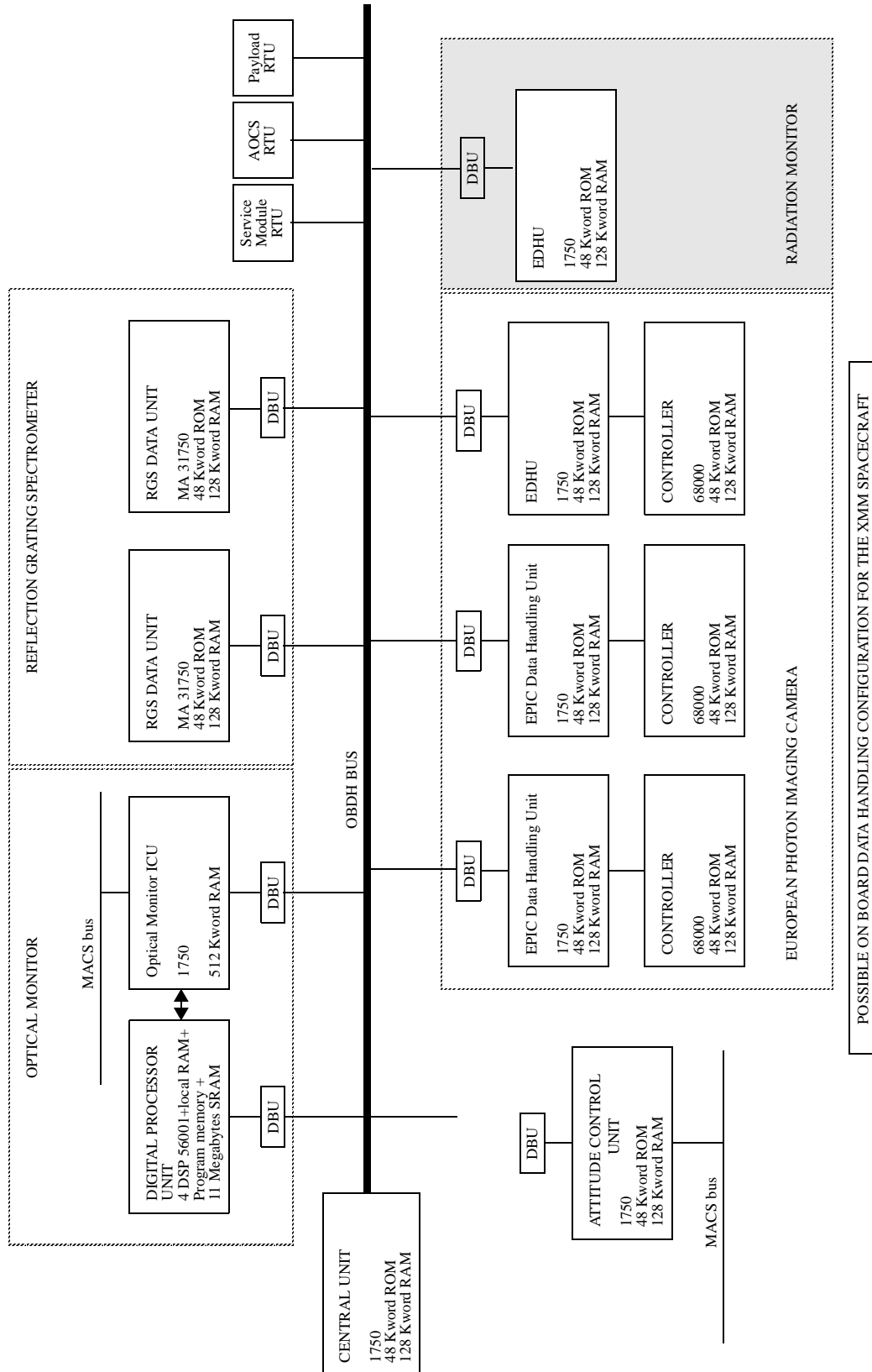
Table 3.

Microprocessor type	Selected chip	Memory size in Kbytes
8 bit microcontroller	TEMIC-MHS 80C32E	64
16 bit microprocessor	MA 31750	256
32 bit RISC	TEMIC-MHS SPARC.RT	1024

For what concerns the memory type selection, the designer can select Rad Hard SRAMs or radiation tolerant SRAMs which are available on the market.

The following diagram represents the availability of the various technologies, along several years.





Analysis of single event upsets effects on a mission

Single event upsets may cause malfunctions in several sensitive functions: microprocessors are affected by bit flips in the microprocessor registers, with immediate effects during the execution of an instruction.

Memory bit flips in the programme code have similar effects.

Bit flips in the data area may have effects on a longer term if no automatic detection and correction are performed.

Bit flips in Input/Output registers may corrupt an address or data in transmitted messages, which is normally detected during protocol verifications.

In terms of criticality, the service interruption of the Spacecraft computers can be described as follows, according to the computer class.

Table 4.

Function	SEU Effects	Corrective action	Prevention in the design
Instrument processors.	<u>Not critical:</u> interruption in an instrument operation loss of mission data.	Reconfiguration of processor possible need for instrument recalibrations.	Protection by EDAC of programme code area is recommended.
Payload processor	<u>Not critical:</u> interruption in a major instrument or several instruments loss of mission data.	Reconfiguration of processor.	HW watchdog protection by EDAC of programme and data area is recommended.
AOCS processor	<u>Highly critical:</u> loss of nominal AOCS. possible loss of Spacecraft safe mode.	Interruption of mission possible automatic protection of sensitive instruments.	HW watchdog Software in ROM, dumped and executed in RAM with EDAC. Hardware survival logic in backup.
Central processor	<u>Critical:</u> interruption of the mission need for the S/C to enter a safety mode.	Interruption of mission operations.	HW watchdog protection by EDAC of programme and data area.

Up to now, Spacecraft design have been efficient enough to limit the SEU effects to mission interruptions only.

Bit flips occurring in microprocessors or code create immediate crashes, which are generally detected by hardware watchdogs.

There is no additional feature required for SEU, since this function is implemented to monitor both hardware and software behaviour.

The watchdog effect is generally a computer restart.

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In order to avoid complete software reloading, the flight software code is often resident in ROM, and copied on to RAM for execution.

This implementation offers the advantage of allowing executable code modifications during the mission.

The implementation choice between Rad Hard chips and Radiation Tolerant components associated to Error Detection and Correction devices (EDACs) depends on several criteria which have to be weighted according to each mission context. The following criteria can be identified:

- Reliability
- Mass
- Size
- Power consumption
- Speed
- Sensitivity to heavy ion
- Error detection capability
- Availability
- Cost

The following chapter details technical design aspects, which allow to establish comparison for these criteria between three implementations for typical microcontroller and microprocessor applications (from 64 to 256 Kbytes memory size).

Solution

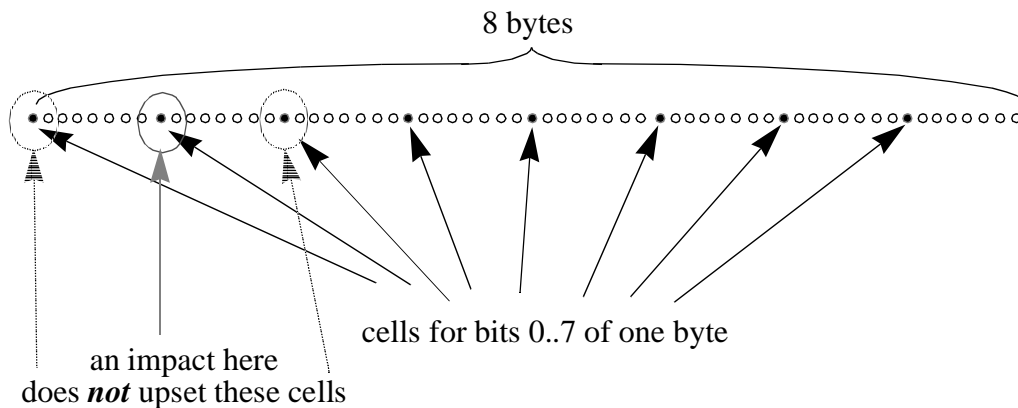
For embedded computer applications where high reliability and autonomy is indispensable, protection of the RAM memory contents is of paramount importance. Such protection is achieved by using Error Detection and Correction (EDAC) circuitry in the hardware design.

EDACs are integrated circuits to be connected to the data bus. The characteristics of an EDAC is to detect and correct single bit errors, and to detect double bit errors (present in one same data word) - this at the expense of

so called check bits added to each data word and a minimum of additional processing.

The TEMIC Matra MHS Static RAM design separates the cells that represent the different dataword bits. This feature virtually eliminates the risk for one impact to provoke dual bit upsets, leaving only a minute risk for single bit upsets - an error that can be detected and corrected by an EDAC.

Figure 1. TEMIC Matra MHS Static RAM Design



The additional processing associated with an EDAC protected solution is the initialisation of the checkbit RAM and a refresh procedure that performs read-write operations on the protected memory ("scrubbing"). The initialisation of the checkbit RAM does not introduce an overhead since most spaceborne applications move their code from ROM to RAM at reset, and automatically initialise the check bit RAM at the same time. The

scrubbing - performed during processor idle time - is necessary to eliminate the risk for two separate impacts to generate a dual bit upset in one same dataword. However, if a dual bit upset in one same data word should occur it would still be detected and signalled by the EDAC.

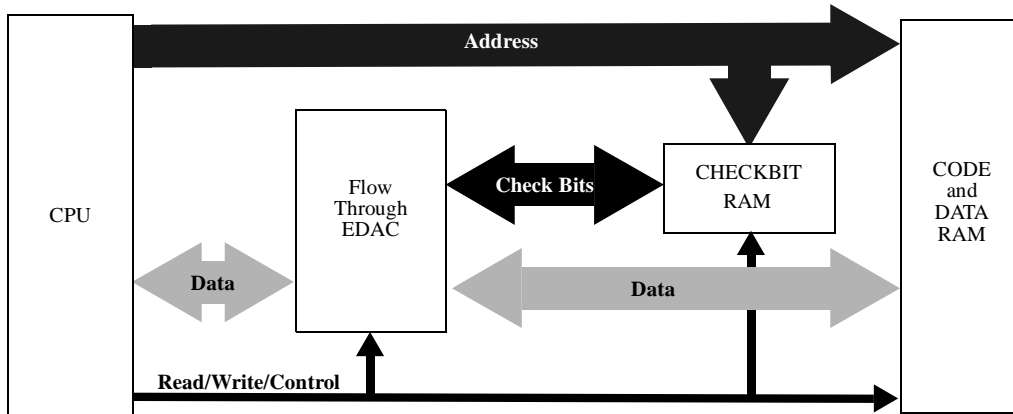
EDAC System Configurations

In a "Correct-Always" system all data passes through the EDAC, where check bits are generated for each write operation and read data is always corrected. To reduce the additional amount of circuitry necessary to

implement this type of system, a flow-through EDAC (separate data buses for CPU and RAM) should be selected.

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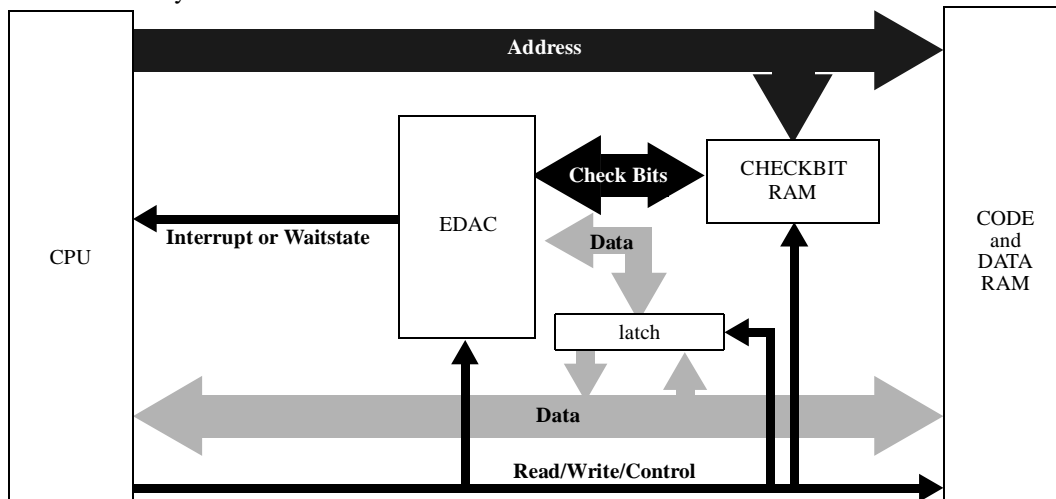
Figure 2. "Correct-Always" system with flow-through EDAC



In a "Bus-Watch" system all write data is fed to RAM and to the EDAC, where check bits are generated. Read data is always checked by the EDAC, and data errors are signalled to the CPU. Flow-through EDACs as well as regular EDACs are suitable for this type of system. The

address with error and the syndrome should be latched to allow correction.

Figure 3. "Bus-Watch" system



The "Bus-Watch" system is suitable for very fast systems, but implies more overhead in the error handling hardware and software. With respect to the processor speeds used in spaceborne systems, the propagation

delay of flow-through EDACs is fast enough and therefore the "Correct-Always" solution has been used for the examples below.

An 8 bit Microcontroller Application

In 8 bit systems, error correction schemes become relatively expensive with respect to the check bits that have to be added - virtually twice the normal memory is required. This example uses the TEMIC-MHS 80C32E, capable of speeds up to 30 MHz, together with TEMIC-

MHS EDAC & RAMs including 64k x 6 bits of additional Check Bit RAM.

The timing diagram shows the External Code Memory Read cycle (fetch) which is more critical than the Data memory read and write cycles.

Table 5. Power & board space consumption for protection of 8 bit application (64 KBytes)

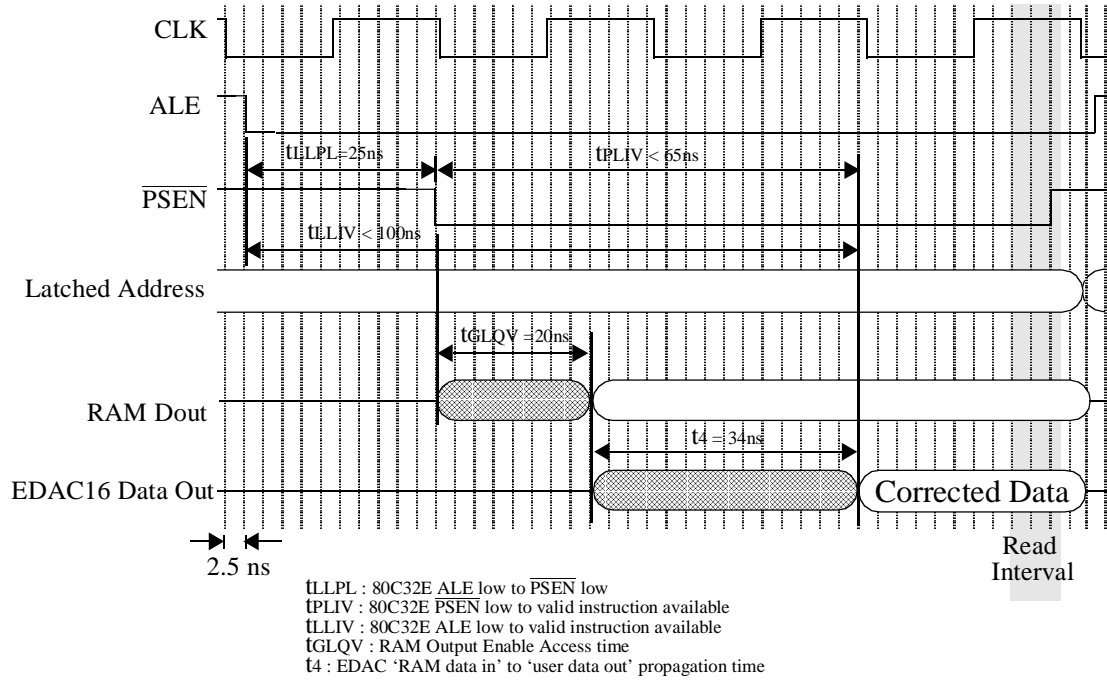
Type of Component	Part count	Flatpack size (mm ²)	- 30 MHz μ C - ICCOP / ICCSB1 (mA)
EDAC: SMKS-29C516E	1	362	20 / 0.02
SRAM 32Kx8RT: SMDP-65656FV-45	4	190	170 / 0.1
Total for 1 st TEMIC-MHS solution ³⁾	5	1122	360 ¹⁾
EDAC: SMKS-29C516E	1	362	20 / 0.02
SRAM 128Kx8RT: SMDI-65608EV-45	2	220	60 / 0.3
Total for 2 nd TEMIC-MHS solution ³⁾	3	802	140 ²⁾
EDAC: SMKS-29C516E	1	362	20 / 0.02
SRAM 32Kx8RH: (45 ns)	4	421	122 / 2
Total for Rad Hard solution ³⁾	5	2046	268 ¹⁾

¹⁾ Two RAMs in operation, two in standby. EDAC

²⁾ Two RAMs in operation. EDAC

³⁾ Not taking into account space board design rules.

Figure 4. TEMIC-MHS80C32E at 30 MHz with TEMIC-MHS 29C516E and SMDP-65656FV-45 (Instr. Read)



Application with 16 bit microprocessor and 64kWords RAM

The example for this application is built around the space qualified MA31750 16 bit microprocessor at 9 or 16 MHz, and TEMIC-MHS EDAC & RAMs including 64K x 6 bits of additional Check Bit RAM.

Table 6. Power and board space consumption for protection of 16 bit application (64 KWords / 128 KBytes)

Type of Component	Part count	Flatpack size (mm ²)	- 9 MHz μ P - ICCOP / ICCSB1 (mA)	- 16 MHz μ P - ICCOP / ICCSB1 (mA)
EDAC: SMKS-29C516E	1	362	20 / 0.02	20 / 0.02
SRAM 32Kx8RT: SMDP-65656FV-45	6	190	65 / 0.1	100 / 0.1
Total for 1 st TEMIC-MHS solution ³⁾	7	1502	215 ¹⁾	320 ¹⁾
EDAC: SMKS-29C516E	1	362	20 / 0.02	20 / 0.02
SRAM 128Kx8RT: SMDI-65608EV-45	3	220	36 / 0.3	45 / 0.3
Total for 2 nd TEMIC-MHS solution ³⁾	4	1022	128 ²⁾	155 ²⁾
EDAC: SMKS-29C516E	1	362	20 / 0.02	20 / 0.02
SRAM 32Kx8RH: (55 ns)	6	421	93 / 2	120 / 2
Total for Rad Hard solution ³⁾	7	2888	305 ²⁾	386 ²⁾

¹⁾ Three RAMs in operation, three in standby. EDAC

²⁾ Three RAMs in operation. EDAC

³⁾ Not taking into account space board design rules.

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No wait state limits clock to 9 MHz

Figure 5. MA31750 at 9MHz with TEMIC-MHS 29C516E and SMDP-65656FV-45 (Read, No wait state)

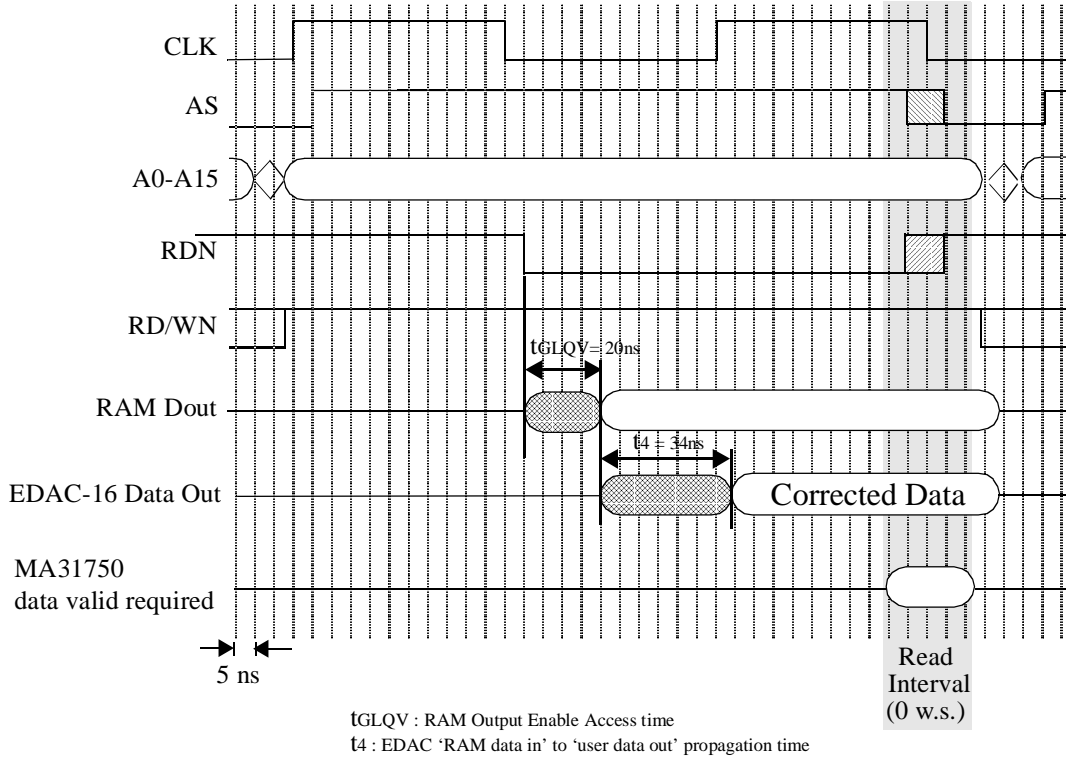
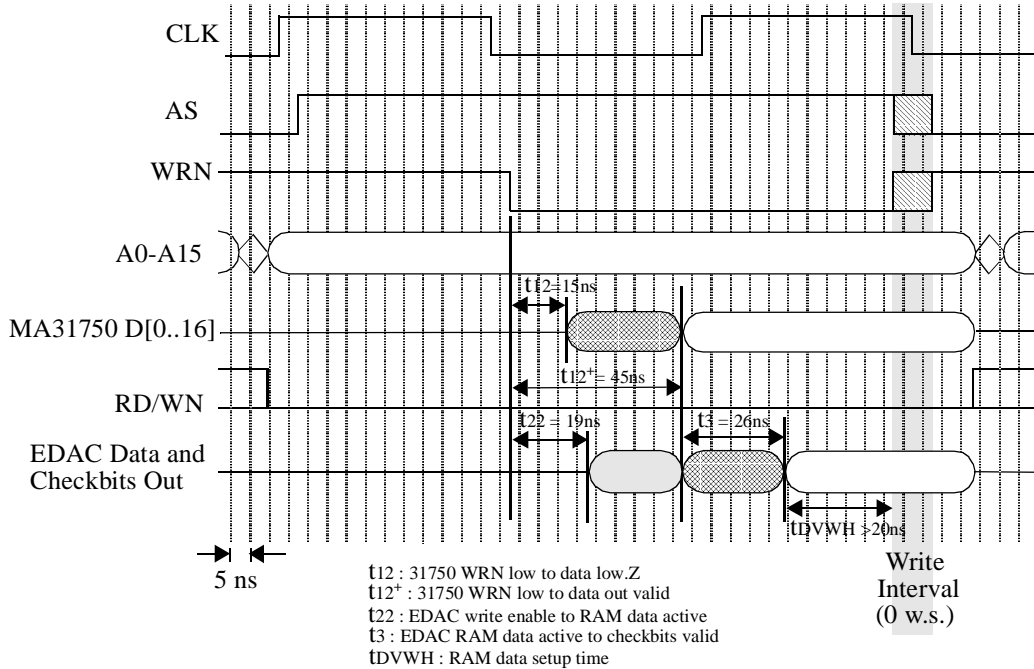


Figure 6. MA31750 at 9MHz with TEMIC-MHS 29C516E and SMDP-65656FV-45 (Write, No wait state)



16 MHz clock speed requires one wait state

Timing analysis at 16 MHz shows that one wait state must be inserted for each memory access cycle with 32K x 8 TEMIC-MHS RAMs - H-65656FV-45.

The increase in execution time due to one wait state in the memory access cycle is estimated to be in the order of 6%.

Figure 7. MA31750 at 16 MHz with TEMIC-MHS 29C516E and SMDP-65656FV-45 (Read, 1 wait state)

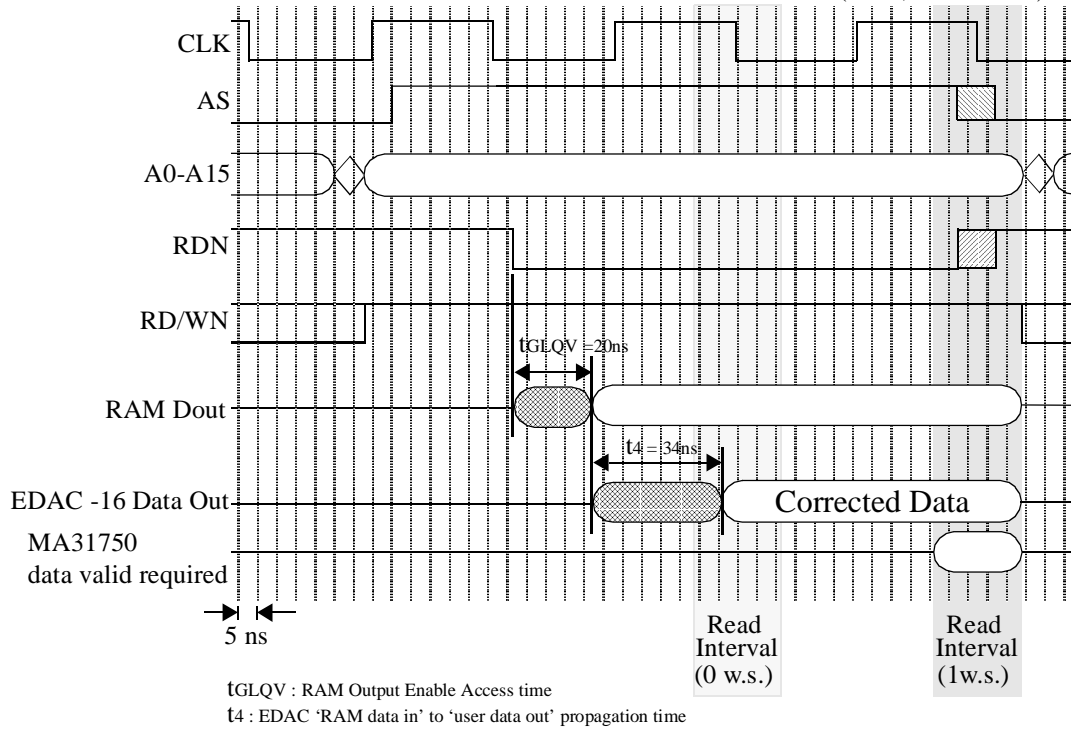
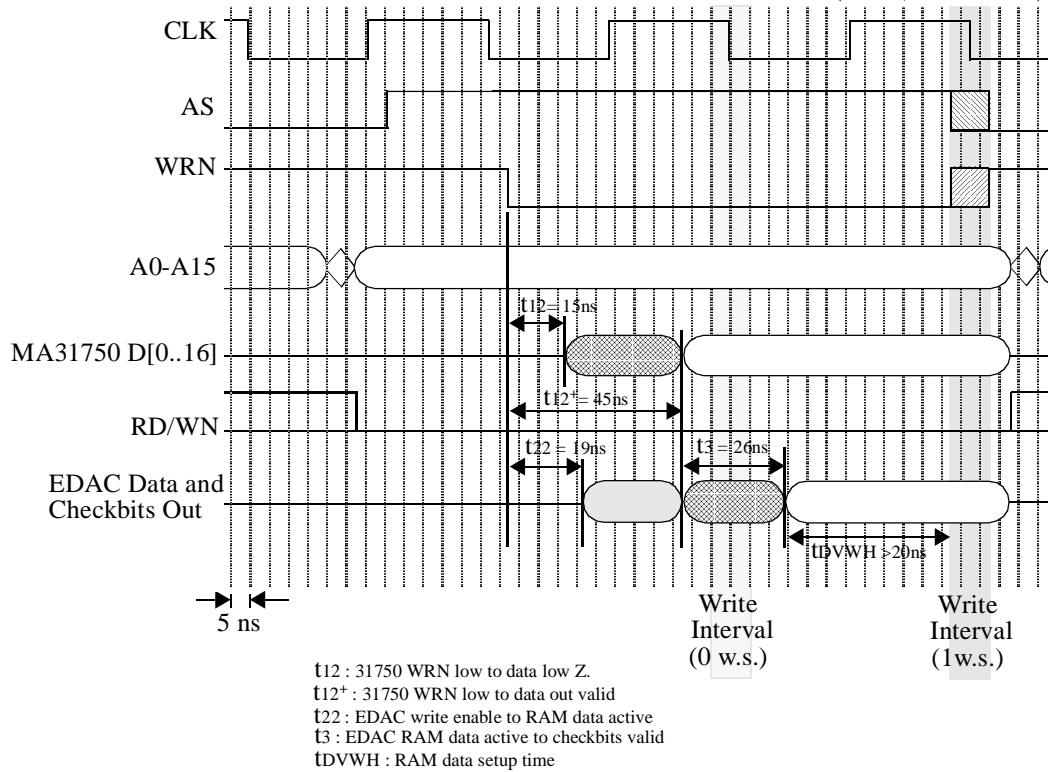


Figure 8. MA31750 at 16 MHz with TEMIC-MHS 29C516E and SMDP-65656FV-45 (Write, 1 wait state)



Application with 16 bit microprocessor and extended memory

The example for this application is built around the space qualified MA31750 16 bit microprocessor and MA31751 memory management unit (MMU) at 16 MHz, TEMIC-MHS EDAC & TEMIC-MHS RAMs including 128Kx6 bits of additional Check Bit RAM.

Table 7. Power and board space consumption for protection of 16 bit application (128 KWords / 256 KBytes)

Type of Component	Part count	Flatpack size (mm ²)	- 16 MHz μ P - ICCOP / ICCSB1 (mA)
EDAC: SMKS-29C516E	1	362	20 / 0.02
SRAM 32Kx8RT: SMDP-65656FV-45	12	190	100 / 0.1
Total for 1 st TEMIC-MHS solution ³⁾	13	2642	321 ¹⁾
EDAC: SMKS-29C516E	1	362	20 / 0.02
SRAM 128Kx8RT: SMDI-65608EV-45	3	220	45 / 0.3
Total for 2 nd TEMIC-MHS solution ³⁾	4	1022	155 ²⁾
EDAC: SMKS-29C516E	1	362	20 / 0.02
SRAM 32Kx8RH: (45ns)	12	421	120 / 2
Total for Rad Hard solution ³⁾	13	5414	398 ¹⁾

¹⁾ Three RAMs in operation, nine in standby. EDAC

²⁾ Three RAMs in operation. EDAC

³⁾ Not taking into account space board design rules.

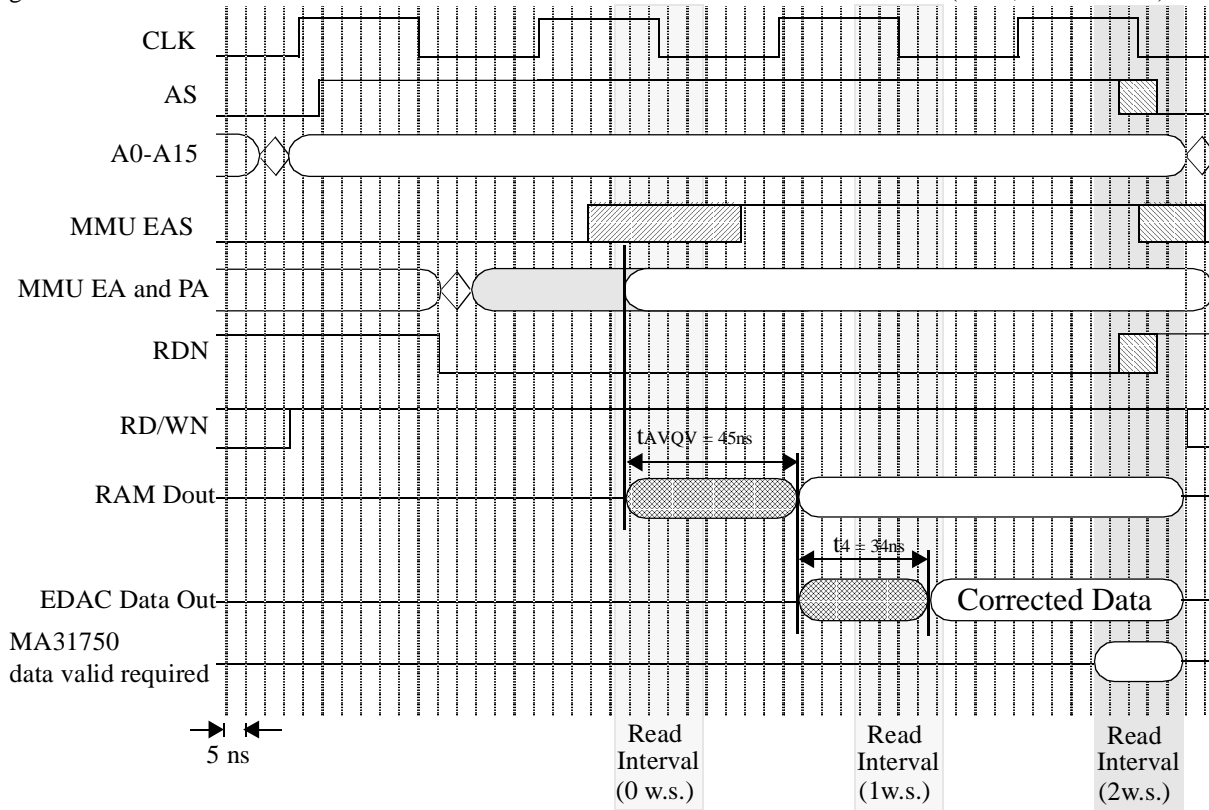
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16 MHz clock requires two wait states

At 16 MHz clock speed, the use of the MMU requires one wait state in the write cycle and two wait states in the read cycle.

The increase in execution time due to the MMU wait states is estimated to be in the order of 20%.

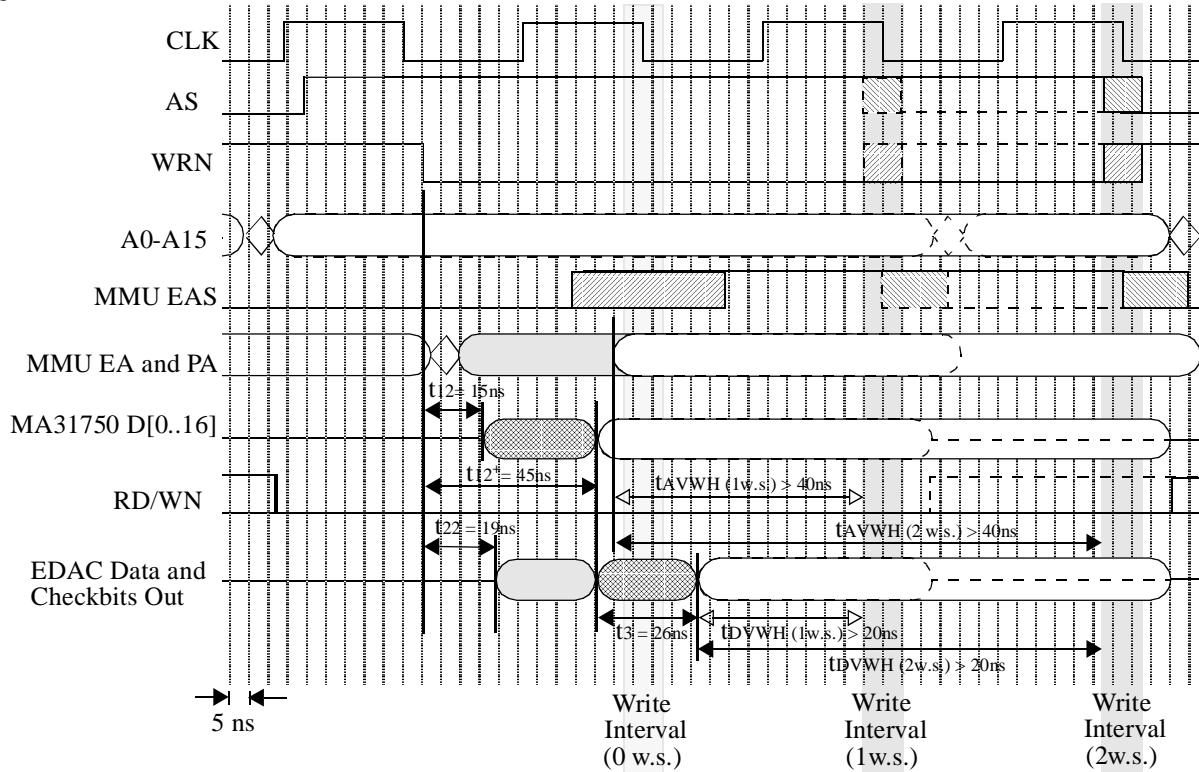
Figure 9. MA31750/51 at 16 MHz with TEMIC-MHS 29C516E and SMDP-65656FV-45 (Read, 2 wait states)



tAVQV : RAM Address Access time

t4 : EDAC 'RAM data in' to 'user data out' propagation time

Figure 10. MA31750 at 16 MHz with TEMIC-MHS 29C516E and SMDP-65656FV-45 (Write, 1 or 2 wait states)



t_{12} : 31750 WRN low to data low Z.
 t_{12}^+ : 31750 WRN low to data out valid
 t_{22} : EDAC write enable to RAM data active
 t_3 : EDAC RAM data active to checkbits valid
 t_{AVWH} : RAM address setup time
 t_{DVWH} : RAM data setup time

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Examples of bit flip predictions for typical computers

Theoretical bit flips for a memory plane based on 256 Kbits memory chips (M-65656F) are the following for a shielding of 5mm (cf RD10 and attached annexes).

Table 8.

Orbit type	Bit flip prediction per bit and per day due to Heavy Ions	Bit flip prediction per bit and per day due to Protons	Total Bit flip prediction per bit and per day
Low Earth Orbit	6.7 E-11	1.6 E-7	1.6 E-7
Polar Orbit	1.6 E-7	4.9E-7	6.5 E-7
Deep Space or Geostationary Orbit	6.2 E-7		6.2 E-7

Table 9. Recalling the two computers detailed in this document :

Computer	Microprocessor type	Selected chip	Memory size in Kbytes
A	8 bit microcontroller	TEMIC-MHS 80C32E	64
B	16 bit microprocessor	MA 31750	256

The bit flips probability to be considered are as follows for inactive and powered chips:

Table 10.

Computer	Memory size in Kilobits	SEU in LEO	SEU in Polar orbit	SEU in Geosynchronous Orbit
A	512	1 per 12.2 days	1 per 3 days	1 per 3 days
B	2048	1 per 3 days	1 per 18 hours	1 per 19 hours

Those figures are for inactive chips, and correspond to the probability of mission interruptions in the absence of any corrective design.

For Low Earth Orbit missions which do not cross the South Atlantic Anomalia (SAA), the M-65656F can be used as such and no need for protection is actually needed.

For all applications in low Earth, Polar and Geosynchronous orbits, protective devices are necessary to limit the impact of SEU on the spacecraft mission.

If an EDAC correction device is added, the necessary memory size is increased due to the correction code

implementation, so the EDAC activation probability is increased.

The SEU probability is given hereunder:

Table 11.

Computer	Memory size in Kilobits	SEU in LEO	SEU in Polar orbit	SEU in Geosynchronous Orbit
A	896	1 per 7 days	1 per 1.7 days	1 per 1.8 days
B	2816	1 per 2.2 days	1 per 13 hours	1 per 14 hours

In terms of occurrence, there is no major difference, but the corrective design based on memory scrubbing has to be performed with a slightly higher frequency.

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Conclusion

The previous analysis allows to conclude that M-65656F can be used for Space applications.

For the most current applications in low earth Orbit, Polar Orbit and Geo-synchronous Orbit, (MA 31750 at 16 MHz using 128 KWords of memory), the use of TEMIC Matra MHS SRAM (M-65656F or M-65608E) with an EDAC (29C516E) appears as a valid solution from a system point of view, at the expense of one additional wait state.

If the processing unit power happened to be actually an issue in an early state of a project, one should consider

that a system problem does exist, which is not likely to be solved at the level of memory chip selection.

For 8 bit microcontrollers in polar Orbit and Geo-synchronous Orbit, using an EDAC means practically to double the memory size, which might have a significant impact on the design. But for such applications, which are non critical, parts costs and availability have to be considered.

Reference documents

This application note is based on a study done by THARSYS in 1994.

- (RD1) **High Reliability Products**, Military and Aerospace Components Data Book, *Matra MHS*, 1993
- (RD2) **8 Bit Microcontrollers**, Data Book, *Matra MHS*, 1993
- (RD3) **80C32/80C52**, Data Sheet, *TEMIC*, 1994
- (RD4) **SOS Radiation Hard**, Hi-Rel IC and ASIC Handbook, *GEC Plessey Semiconductor*, 1993
- (RD5) **16 Bits EDAC**, Product Specification, *Saab Ericsson Space*, 1993
- (RD6) **Detect/Correct Errors to improve data reliability**, A. Hegde (IDT), *Electronic Design*, Vol 40, No 12, 11/6/1992
- (RD7) **Designing with the IDT49C460 and IDT39C60 Error Detection and Correction Units**, Application Note AN-24, *Integrated Device Technology, Inc.*, 1989
- (RD8) **High Performance Logic**, Data Book, *Integrated Device Technology, Inc.*, 1992
- (RD9) **Radiation Hardened 32kx8 SOI CMOS Static RAM**, Data Sheet, *Harris Semiconductor*, 12/1992
- (RD10) **Evaluation of Heavy Ions and Protons induced upset rates of HM-65664E and M-65656F TEMIC Matra MHS static RAMs** (*HIRES Technical Note, HRX/93.276, 26/11/93*).

Annexes

Examples from (RD10) **Evaluation of Heavy Ions and Protons induced upset rates of HM-65664E and M-65656F TEMIC Matra MHS static RAMs** (*HIREX Technical Note, HRX/93.276, 26/11/93*).

